

CLAIMS

1. (Previously presented) An automatic phase and frequency adjust circuit, comprising:
 - a phase locked loop circuit to generate a phase locked loop clock responsive to a reference signal;
 - an edge detector circuit to generate an edge pulse signal corresponding to a transition of an analog data signal responsive to a pixel clock;
 - a phase detector circuit to generate a phase adjust signal responsive to a phase of the phase locked loop clock and the edge pulse signal; and
 - a phase adjust circuit to generate the pixel clock responsive to the phase adjust signal and the phase locked loop clock.
2. (Original) The automatic phase and frequency adjust circuit of claim 1 wherein the phase locked loop circuit comprises:
 - a phase detector adapted to receive the reference signal;
 - a loop filter coupled to the phase detector;
 - a voltage controlled oscillator coupled to the loop filter;
 - a feedback loop adapted to receive the phase locked loop clock and provide a feedback signal responsive to a frequency adjust signal.
3. (Original) The automatic phase and frequency adjust circuit of claim 1 wherein the reference signal is a horizontal synchronization signal.
4. (Previously presented) The automatic phase and frequency adjust circuit of claim 1 wherein the edge detector generates an edge pulse corresponding to the transition of the analog data signal above a predetermined threshold.
5. (Original) The automatic phase and frequency adjust circuit of claim 4 wherein the threshold is programmable.
6. (Previously presented) The automatic phase and frequency adjust circuit of claim 1 wherein the edge detector generates an edge pulse corresponding to a rising, falling, or both rising and falling edges of the analog data signal.

7. (Previously presented) The automatic phase and frequency adjust circuit of claim 1 wherein the phase adjust circuit adjusts the phase of the pixel clock by delaying the reference signal.

8. (Previously presented) The automatic phase and frequency adjust circuit of claim 1 wherein the phase adjust circuit adjusts the phase of the pixel clock by delaying the phase locked loop clock.

9. (Previously presented) The automatic phase and frequency adjust circuit of claim 8 wherein the phase adjust circuit comprises:

a clock delay circuit to generate a plurality of delayed clock signals by delaying the phase locked loop clock; and

a multiplexer to select one of the plurality of delayed clock signals as the pixel clock responsive to a phase adjust signal.

10. (Original) The automatic phase and frequency adjust circuit of claim 9 wherein the clock delay circuit comprises an n-stage delay locked loop, each stage generating a corresponding delayed clock phase, each delayed clock phase being $360/n$ degrees out of phase.

11. (Previously presented) The automatic phase and frequency adjust circuit of claim 1

wherein the phase adjust circuit generates a plurality of delayed clock signals by delaying the phase locked loop clock; and

wherein the phase detector comprises:

a phase hit detector to generate a plurality of phase hit enable signals corresponding to the plurality of delayed clock signals and assert one of the phase hit enable signals responsive to the edge pulse signal; and

a phase hit counter to count asserted phase hit enable signals for each of the delayed clock signals over a predetermined time.

12. (Original) The automatic phase and frequency adjust circuit of claim 11 wherein the predetermined time is a number of image scan lines.

13. (Previously presented) The automatic phase and frequency adjust circuit of claim 11 wherein the phase hit detector comprises:

a plurality of flip-flop circuits corresponding to the plurality of delayed clock signals to generate a corresponding plurality of phase out signals; and
a comparison circuit to comparing the plurality of phase out signals.

14. (Previously presented) The automatic phase and frequency adjust circuit of claim 13 wherein the comparison circuit compares adjacent phase out signals.

15. (Previously presented) The automatic phase and frequency adjust circuit of claim 11 wherein the phase hit counter comprises:

an enable signal to enable counting of asserted phase hit enable signals; and
a clear signal to clear the phase hit counter.

16. (Previously presented) The automatic phase and frequency adjust circuit of claim 11 comprising:

a phase count analysis circuit to generate phase and frequency adjust signals by analyzing the count of asserted phase hit enable signals.

17. (Previously presented) The automatic phase and frequency adjust circuit of claim 1 comprising an auto calibration circuit to align the analog data signal with the pixel clock.

18. (Previously presented) A circuit, comprising:

an edge detector to generate an edge pulse corresponding to a transition of an analog image signal responsive to a pixel clock;

a phase adjust circuit to generate the pixel clock by selecting one of a plurality of phases of a phase locked loop clock responsive to a phase adjust signal; and

a phase detector circuit to generate the phase adjust signal responsive to the edge pulse signal.

19. (Previously presented) The circuit of claim 18 wherein the edge detector generates the edge pulse signal responsive to a transition of the analog signal greater than a predetermined threshold.

20. (Previously presented) The circuit of claim 18 wherein the edge detector generates the edge pulse responsive to a rising, falling, or both rising and falling edges of the analog image signal.

21. (Original) The circuit of claim 18 wherein the edge detector comprises a calibration circuit adapted to calibrate the analog image signal with the pixel clock.

22. (Previously presented) The circuit of claim 18 wherein the phase adjust circuit generates the pixel clock by delaying a reference signal.

23. (Previously presented) The circuit of claim 18 wherein the phase adjust circuit comprises:

a delay locked loop to generate the plurality of clock phases by delaying the phase locked loop clock; and

a multiplexer to select one of the plurality of delayed clock signals as the pixel clock responsive to the phase adjust signal.

24. (Original) The circuit of claim 23 wherein the delay locked loop includes n stages, each clock phase being $360/n$ degrees out of phase.

25. (Previously presented) The circuit of claim 18 wherein the phase adjust circuit comprises a clock delay circuit to generate the plurality of clock phases by delaying the phase locked loop clock signal; wherein the phase detector circuit comprises:
a phase hit enable signal corresponding to each of the plurality of clock phases, the phase hit enable signal being asserted responsive to the edge pulse signal;
a count corresponding to each of the plurality of clock phases, the count being indicative of a number of assertions of a corresponding phase hit enable signal over a predetermined time.

26. (Previously presented) The circuit of claim 25 wherein the phase detector circuit comprises:
an enable signal to enable the phase detector circuit; and
a clear signal to clear each count.

27. (Original) The circuit of claim 25 wherein the predetermined time is a number of image scan lines.

28. (Previously presented) The circuit of claim 25 wherein the phase detector circuit generates the phase adjust signal by analyzing the count.

29. (Previously presented) The circuit of claim 25 comprising a phase locked loop circuit to derive the phase locked loop clock signal from a reference signal responsive to a frequency adjust signal.

30. (Previously presented) The circuit of claim 29 wherein the phase detector circuit generates the phase and frequency adjust signals by analyzing each count.

31. (Previously presented) A method for automatically adjusting a phase and frequency of a pixel clock in a digital image system, comprising:

generating a plurality of clock phases by delaying a phase locked loop clock signal by a plurality of delays;

detecting a transition of an analog image signal responsive to a pixel clock signal;

determining which of the plurality of clock phases corresponds to the transition by substantially simultaneously comparing the transition to the plurality of clock phases;

asserting a clock phase hit responsive to the determining;

counting a number of clock phase hits for each of the clock phases; and

generating a phase and frequency adjust signal as a result of the counting.

32. (Previously presented) The method of claim 31 comprising deriving the phase locked loop clock signal from a reference signal responsive to the frequency adjust signal.

33. (Original) The method of claim 31 comprising selecting a clock phase as the pixel clock responsive to the phase adjust signal.

34. (Original) The method of claim 31 wherein detecting a transition includes detecting a transition of the analog image signal above a predetermined threshold.

35. (Original) The method of claim 31 wherein detecting a transition includes detecting a rising, falling, or both rising and falling edges of the analog image signal.

36. (Previously presented) The method of claim 31 wherein detecting a transition includes generating an edge pulse responsive to the transition and wherein asserting a clock phase hit includes comparing the edge pulse with each of the clock phases.

37. (Original) The method of claim 31 wherein asserting the clock phase hit includes generating a plurality of clock phase hit signals corresponding to the plurality of clock phases and asserting only the clock phase hit signal closest to the transition.

38. (Original) The method of claim 31 wherein counting the number includes counting the number of clock phase hits for each of the clock phases over a predetermined time.

39. (Original) The method of claim 38 wherein the predetermined time is a number of image scan lines.

40. (Previously presented) The method of claim 38 wherein counting includes:
clearing the counting; and
enabling the counting.

41. (Previously presented) The method of claim 38 wherein counting includes generating a count for each of the clock phases and wherein counting comprises:
examining the count; and
adjusting the frequency of the pixel clock if the count exceeds a predetermined number.

42. (Previously presented) The method of claim 41 wherein adjusting the frequency of the pixel clock comprises:
changing the frequency of the phase locked loop clock signal;
clearing the count;
enabling the count;
repeating the counting, examining, and adjusting if the count exceeds a predetermined number.